How to use the DDS RF Source

1. Connect via a *crossover* Ethernet cable to the Rabbit.

2. Plug in both of the power supplies.

3. Make sure that the FPGA is on.

4. Run **RabbitCom\_dbg.exe**

Currently at \\Orchid\common\JH\_FPGA\_WORK\_8-23-10\rabbit gui\RabbitCom\_dbg.exe

5. Click on **DDS Initial Setup .**

6. Type the limits and sweep time you want for the first sweep and click **Send.**

7. Repeat step 6 for all additional sweeps.

8. Click **Finalize.**

9. Now trigger each sweep by sending a TTL pulse to the **TRG** jack on the box.

-Each sweep starts approximately 42.2μs after the trigger.

-Occasionally, the first time you do a sweep, nothing (or something unwanted) will happen; therefore, the DDS and/or the FPGA will need to be restarted.

10. Repeat steps 5 through 9 for each additional set of sweeps.

How to load the program onto the Rabbit

1. Open Dynamic C 9.21

2. Open the file AD9910\_SWEEP\_JH\_EDIT.C

Currently it is located \\Orchid\common\ J\_H\_FPGA\_WORK\_8-23-10\rabbit dyn c file\ AD9910\_SWEEP\_WAYSTATION\_JH\_EDIT.C

3. Connect the Programming Cable to the Rabbit, as shown below, and the computer’s ***COM Port (10101),*** *not* the USB port as shown in the picture below.



-Sometimes the header from the cable needs to be taken off and reinserted for it to accept the connection for some reason

4. Make sure the Rabbit is powered

5. Compile the program in Dynamic C. The computer must be connected to the powered up Rabbit for this to work

6. Make sure the Ethernet crossover cable is connected.

7. Run program in Dynamic C.

- A dialog box will come up that states “Listening for a connection.”

-Also, 2 green lights will light up on the Rabbit next to the Ethernet port, and a yellow one when data is being sent to the Rabbit

8. Now you can run the program(GUI), RabbitCom\_dbg.exe, as shown above. The progress of this interchange is shown in the dialog box when this program in running Dynamic C.

9. To have the Rabbit operate this program as a “stand-alone,” unplug the Programming Cable and power down and power up the Rabbit.

How to load/edit the program on the FPGA

1. The program being used for the FPGA in the RF source is currently located at \\Orchid\common\J\_H\_FPGA\_WORK\_8-23-10\RABBIT\_DDS\_FIFO(final)\

2. Open any version of Quartus II. This program was written with Quartus II 7.1.

3. Open RABBIT\_DDS\_FIFO.cdf

4. A tutorial to get started using Quartus II with Verilog HDL for programming the FPGA is currently on the web at <http://saaubi.people.wm.edu/TeachingWebPages/Physics351_Fall2009/Week2/tut_quartus_intro_verilog.pdf>. This will give a detailed explanation on how to use Quartus II and program the FPGA.+